REMARKS

Claims 1-19 of the present application remain pending. Claims 17, 18, and 19 are amended herein. Applicants respectfully submit that no new matter is added as a result of the claim amendments.

CLAIM REJECTIONS 35 U.S.C. § 102

Claims 1-19 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kobayashi et al (U.S. Patent No. 6,199,091), hereinafter referred to as "Kobayashi." The Applicants respectfully submit that these claimed embodiments of the present invention are not anticipated or suggested by Kobayashi. Claim 1 of the present invention is directed to a method of performing a pipelined arithmetic function and recites (emphasis added):

> a) receiving two N-bit operands into each of a plurality of adder elements in separate pipelines;
>
> b) performing an add operation in each of said plurality of adder elements wherein a first N-bit result and a first carry bit is output from each of said adder elements;
>
> c) receiving said first N-bit result from each of said adder elements into a respective N-bit result register and receiving said first carry bit from each of said adder elements into a respective carry bit register;
>
> d) outputting from an incrementor in one of said pipelines, a second N-bit result and a second carry bit from the combination of a first result from a first of said N-bit result registers, a first carry bit from a first of said carry bit registers, and a first carry bit from a second of said carry bit registers from a second of said pipelines; and
>
> e) supplying a final result being a combination of said second N-bit result from said incrementor, said second carry bit from said incrementor, and said first N-bit result from a second N-bit result register in said second pipeline.

The embodiments of Claims 8 and 16 are directed to a pipelined adder/subtractor and a multistage adder/subtractor respectively and recite similar claim limitations. The Applicants respectfully submit that Kobayashi does not teach or suggest the claim limitation recited in embodiments of the present invention of (emphasis added):

a) receiving two N-bit operands into each of a plurality of adder elements in separate pipelines;

The Applicants respectfully submit that Claim limitations recited in Claims 1, 8, and 16 are inconsistently defined when applied to the cited art. Thus, the rejection selectively defines the term "N-bit operand" in order to selectively fit the recited limitations of the present invention. The rejection states that Kobayashi teaches a first adder which yields Z0-Z2 in a separate pipeline and a second adder which yields Z3-Z8 in a separate pipeline. However, the operands input to the first adder are 3-bit operands (e.g., N=3) while the operands input to the second adder are 6-bit operands (e.g., N=6). The Applicants respectfully submit that inconsistently defining the term "N-bit operand" results in an unreasonably broad interpretation of the recited Claim limitations.

Furthermore, the rejection states that X and Y operands of Kobayashi are N-bit operands. Thus, in Figure 1 of Kobayashi, X and Y are 16-bit operands. The Applicants respectfully submit that Kobayashi does not teach receiving two N-bit operands into each of plurality of adder elements in separate pipelines. As stated above, the rejection states that the first pipelined adder yields Z0-Z2, while the second pipelined adder yields Z3-Z8. However, neither the first or second adder of Kobayashi receives a 16-bit operand. Instead, portions of each of the two 16-bit

operands are distributed among the separate combinatorial pathways. The Applicants further submit that the term "N-bit operand" is again defined inconsistently when applied to Kobayashi. As discussed above, the term "N=bit operand" was selectively defined (e.g., N= 3, or N=4), depending upon which adder was being cited. However, now the rejection implies that X and Y are 16-bit operands (e.g., N=16). The Applicants again assert that inconsistently defining the term "N-bit operand" results in a misinterpretation of the claim limitation recited in Claims 1, 8 and 16 of the present invention. The Applicants therefore respectfully submit that the embodiments of the present invention recited in independent Claims 1, 8, and 16 are not anticipated by the teaching Kobayashi which distributes portions of the N-bit operands among the pathways and that the rejections under 35 U.S.C. § 102(e) are overcome.

The Applicants further submit that Kobayashi does not teach or suggest the claim limitation recited in embodiments of the present invention of (emphasis added):

> b) performing an add operation in each of said plurality of adder elements wherein a first N-bit result and a first carry bit is output from each of said adder elements;

The Applicants again assert that the inconsistent definition of the term "N-bit" operand" results in a misinterpretation of the claim limitations recited in Claims 1, 8, and 6 of the present invention. As described above, the rejection cites the Z0-Z2 as comprising a first pipeline and Z3-Z8 as comprising a second pipeline. As discussed above, in Figure 1 of Kobayashi, X and Y are both 16 bit operands, thus, N=16. However, the first pipeline cited in the rejection only outputs a 3 bit result while the second pipeline outputs a 6 bit result and the third pipeline outputs a 7 bit operand. Thus, the Applicants respectfully submit that Kobayashi teaches away from

embodiments of the present invention which recite that each of the adder elements in each pipeline receives two N-bit operands and outputs an N-bit result. Accordingly, the Applicants respectfully submit that the embodiments of the present invention recited in independent Claims 1, 8, and 16 are not anticipated by the teaching of Kobayashi which does not output an N-bit result from each of the adder elements and that the rejections under 35 U.S.C. § 102(e) are overcome.

The Applicants further submit that Kobayashi does not teach or suggest the claim limitation recited in embodiments of the present invention of (emphasis added):

> c) receiving said first N-bit result from each of said adder elements into a respective N-bit result register and receiving said first carry bit from each of said adder elements into a respective carry bit register;

The rejection states the implicit existence of registers to store the results for Z0-Z2 despite the clear circuit diagrams of this cited art that explicitly do not teach or suggest their existence. Specifically, Kobayashi does not specifically teach or suggest storing the results of Z0-Z2 in a register whose contents are used in another pipeline. For example, Figure 1 of Kobayashi does not show or suggest that the result from an adder element is received in a respective result register. Furthermore, Kobayashi does not teach or suggest that the results from the other adder elements (e.g., Z3-Z8, and Z9-Z15) are stored in result registers. The rejection states that it is inherent that the result is output to a result register. The Applicants respectfully disagree with this assertion as the results from each adder element (e.g., {3,5}, {7,9}, {11,13}, etc.) are directly input to further combinatorial logic as shown in Figure 1. The circuit pathways of the

cited art are well known combinatorial logic gates which do not provide a stage function of any sort Furthermore, Kobayashi does not teach or suggest the existence of a register of any sort. Therefore, the Applicants respectfully assert that the assumption that Kobayashi teaches or suggests storing the N-bit result in respective N-bit result registers, as recited in Claims 1, 8, and 16 of the present invention, is not supported in the cited art and is misplaced.

Nor does Kobayashi teach or suggest the recited claim limitation of receiving said first carry bit from each of said adder elements into a respective carry bit register. Instead, the carry bits of the apparatus shown by Kobayashi (e.g., C1, C3, and C4) are direct inputs into the combinatorial logic of other pathways without first being held in a register or storage unit of any kind. Again, the rejection states that it is inherent that the carry bit be output to a carry bit register. The Applicants respectfully submit that this is refuted by Kobayashi because carry bits C1, C2, C3, and C4 are directly input into additional combinatorial logic, not carry bit registers. More specifically, carry bits C1, C2, and C3 are respectively input directly into a plurality of AND gates and an XOR gate. Accordingly, the Applicants respectfully assert that the statement that it is inherent that the carry bit be output to a carry bit register is not supported by the cited art and ignores the clear meaning of these claim limitations.

Furthermore, in teaching that the carry bits C1, C2, and C3 are respectively input directly into a plurality of AND gates and an XOR gate, the Applicants respectfully submit that Kobayashi teaches away from the claim limitations recited in Claims 1, 8, and 16 of the present invention. Thus, the Applicants respectfully submit that the embodiments of the present

invention recited in independent Claims 1, 8, and 16 are not anticipated by the teaching Kobayashi which does not store an N-bit result from each adder element in a respective N-bit register and which does not receive a carry bit from each of the adder elements into a respective carry bit register. Therefore, the Applicants respectfully submit that the rejections under 35 U.S.C. § 102(e) are overcome.

The Applicants assert that Kobayashi does not teach result registers and carry bit registers because Kobayashi's design is not pipelined, as claimed, but rather is purely combinatorial. Therefore, the cited art has no need to register data from one clock cycle to the next. For instance, Kobayashi does not teach use of clocked pipestages within a pipeline where the results of one clocked pipeline are fed to a downstream pipestage via clocked registers over different clock cycles. Kobayashi's circuit is merely one combinatorial circuit pathway that operates within a common clock cycle. Additionally, Kobayashi does not teach or suggest a clock signal for regulating clocked pipestages, or the registeres that are required to pass data from one clock cycle to the next. Therefore, because the apparatus of Kobayashi does not require result registers and/or carry bit registers, these elements are not taught nor suggested by Kobayashi.

The Applicants respectfully submit that Kobayashi does not teach or suggest the recited claim limitation of (emphasis added):

> d) outputting from an incrementor in one of said pipelines, a second N-bit result and a second carry bit from the combination of a first result from a first of said N-bit result registers, a first carry bit from a first of said carry bit registers, and a first carry bit from a second of said carry bit registers from a second of said pipelines;

The Applicants respectfully submit that Kobayashi does not teach or suggest an incrementor of any sort. While the rejection cites the combinatorial logics in the lower portion of the pipeline producing Z3-Z4, except 7 and 9, as comprising an incrementor, Kobayashi does not teach or suggest that the function of an incrementor is performed by these logic elements or other elements shown in Figures 1-4. Additionally, the Applicants respectfully submit that combinatorial logic in the lower portion of the pipeline producing Z3-Z4 is not operable as an incrementor as described in the present application.

With reference to Figure 4 of the present invention, an incrementor as recited in Claims 1, 8, and 16 is clearly described.

The function of an incrementor utilized in embodiments of the present invention is shown in greater detail in Figure 4. For purposes of clarity, reference will be made to Figure 4 and to incrementor 225 of Figure 2. Incrementor 400 is comprised of a simple incrementor 410 and an OR gate 430. Incrementor 400 receives a first result into incrementor 410 from an adder element in its respective pipeline (e.g., adder element 220 of Figure 2) as well as a first carry bit from a second adder element (e.g., adder element 210 of Figure 2) in a different pipeline. Adder 410 performs an increment operation and outputs a second result and, if necessary, a carry bit.

The carry bit is input into OR gate 430 along with the first carry bit from the adder element 220. OR gate 430 performs a Boolean OR operation and outputs a second carry bit to carry bit register 440 (e.g., carry bit register 227 of Figure 2). It is appreciated that in some embodiments of incrementor 400 the second result and second carry bit may be directly input into output bus 250 (e.g., incrementor 248 of Figure 2). In other embodiments of incrementor 400, the second result and the second carry bit are stored in pipelined registers (e.g., registers 226 and 227 of Figure 2).

The Applicants respectfully submit that the combinatorial logic of Kobayashi is not operable to perform the operation of an incrementor as described above. For example, incrementor 410 outputs a carry bit directly to an OR gate (e.g., 430) which also receives a current stage

add/subtract bit. In the apparatus of Kobayashi, a carry bit (e.g., the output from adder 7 which is not input into adder 9) is directly input into a plurality of AND gates and an XOR gate. Thus, the apparatus taught by Kobayashi teaches away from the claim limitations recited in Claims 1, 8, and 16 of the present invention. Accordingly, the Applicants respectfully submit that the embodiments of the present invention recited in independent Claims 1, 8, and 16 are not anticipated by the teaching Kobayashi and that the rejections under 35 U.S.C. § 102(e) are therefore overcome.

The Applicants respectfully submit that the embodiments of the present invention recited in Claims 1 and 8 recite a pipelined arithmetic function and a pipelined adder/subtractor respectively. Claim 17 recites a plurality of pipelines, each of which is divided into clock regulated pipestages. The Applicants respectfully submit that it is well known by one skilled in the relevant art that a pipelined arithmetic function and a pipelined adder/subtractor also refer to an implementation which utilizes clock regulated pipestages. The Applicants respectfully submit that Kobayashi does not teach or suggest that clock regulated stages are used in any manner. Instead, the combinatorial adders and associated logic shown by Kobayashi are not regulated by any type of pipelined clock cycle, or as a series of clock cycles. Accordingly, the Applicants respectfully submit that the embodiments of the present invention recited in independent Claims 1, 8, and 16 are not taught or suggested by Kobayashi and that the rejections under 35 U.S.C. § 102(e) are overcome.

With reference to Claims 2, 9, 12, 14, and 17, the rejection states that Kobayashi teaches the use of single width registers. The Applicants respectfully submit that Kobayashi does not teach or suggest the use of any sort of register, much less the use of single width registers as recited in Claims 2, 9, 12, 14, and 17. Accordingly, the Applicants respectfully submit that the rejection of Claims 2, 9, 12, 14, and 17 under 35 U.S.C. § 102(e) are overcome.

With reference to Claims 3, and 10, the rejection states that Kobayashi teaches the use of single bit registers for a carry bit. The Applicants respectfully submit that because Kobayashi does not have a pipelined system, it does not teach or suggest the use of any sort of register, much less the use of single bit registers for a carry bit as recited in Claims 3, and 10. Accordingly, the Applicants respectfully submit that the rejection of Claims 3, and 10 under 35 U.S.C. § 102(e) are overcome.

With reference to Claims 4, and 11 the rejection states that Kobayashi teaches receiving a first N-bit result into a plurality of single width N-bit registers. The Applicants respectfully submit that Kobayashi does not teach or suggest the use of any sort of register, much less the use of single width N-bit registers recited in Claims 4, and 11. While the rejection cites box 7 as teaching a single width register, Kobayashi teaches in column 7, line 10, that box 7 comprises a half adder. Therefore the Applicants respectfully submit that the cited art does not teach or suggest the claim limitation recited in Claims 4, and 11 of the present invention. Accordingly, the Applicants respectfully submit that the rejection of Claims 4, and 11 under 35 U.S.C. § 102(e) are overcome.

With reference to Claim 5, the rejection states that Kobayashi teaches respectively receiving a first carry bit into a plurality of single bit registers. The Applicants respectfully submit that Kobayashi does not teach or suggest the use of any sort of register, a carry bit register of any sort, or much less the use of single bit registers as recited in Claim 5. As described above, Kobayashi teaches that bit C1 is directly input into a plurality of AND gates and an XOR gate, thus teaching away from the claim limitation recited in Claim 5 of the present invention. Accordingly, the Applicants respectfully submit that the rejection of Claim 5 under 35 U.S.C. § 102(e) is overcome.

With reference to Claims 6, 13, and 18 the rejection states that Kobayashi teaches respectively receiving a N-bit result into a plurality of single width N-bit registers. As described above, the Applicants respectfully submit that Kobayashi does not teach or suggest the use of any sort of register, much less the use of single width N-bit registers as recited in Claims 6, 13, and 18. Accordingly, the Applicants respectfully submit that the rejection of Claims 6, 13, and 18 under 35 U.S.C. § 102(e) are overcome.

With reference to Claim 7, the rejection states that Kobayashi teaches respectively receiving a second carry bit into a plurality of single bit registers. As described above with reference to Claim 5, the Applicants respectfully submit that Kobayashi does not teach or suggest the use of any sort of register, a carry bit register of any sort, or the use of single bit registers as recited in Claim 7. As described above, Kobayashi teaches that bit C2 is directly

input into a plurality of AND gates and an XOR gate, thus teaching away from the claim limitation recited in Claim 7 of the present invention. Accordingly, the Applicants respectfully submit that the rejection of Claim 7 under 35 U.S.C. § 102(e) is overcome.

With reference to Claims 15 and 19, the rejection states that Kobayashi teaches a plurality of carry bit registers for respectively receiving carry bits from adder elements and an incrementor. As described above with reference to Claim 5, the Applicants respectfully submit that Kobayashi does not teach or suggest the use of any sort of register, a carry bit register of any sort, or an incrementor as recited in Claims 15 and 19. As described above, Kobayashi teaches that bit C2 is directly input into a plurality of AND gates and an XOR gate, thus teaching away from the claim limitation recited in Claims 15 and 19 of the present invention. Accordingly, the Applicants respectfully submit that the rejection of Claims 15 and 19 under 35 U.S.C. § 102(e) is overcome.

CONCLUSION

Based on the arguments presented above, the Applicants respectfully assert that Claims 1-19 overcome the rejections of record and, therefore, the Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

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Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060